CLAIMS

What is claimed is:

1. In the fabrication of a three dimensional memory where memory cells are formed at the intersection of generally parallel, spaced-apart rail-stacks disposed at a plurality of rail-stack levels, an improvement wherein the depth of etching in at least two etching steps used to form the rail-stacks in two adjacent rail-stack levels is approximately equal.

2. The improvement defined by claim 1, wherein each of the two etching steps etches a plurality of layers used to form the rail-stacks at one level of rail-stacks, and additionally partially etches rail-stacks in an underlying adjacent level of rail-stacks so as to form pillar structures in the underlying adjacent level of rail-stacks.

3. The improvement defined by claim 2, wherein the pillar structures comprise N- regions of silicon.

4. The improvement defined by claim 3, wherein the N- regions associated with diodes in the memory cells.

5. The improvement defined by claim 4, wherein the memory cells include an antifuse regions.

6. The improvement defined by claim 2, wherein the pillar structures are associated with diodes in the memory cells.

7. The improvement defined by claim 6, wherein the memory cells include antifuse regions.

8. A three dimensional memory array comprising:

a plurality of memory level pairs;

each memory level pair including a plurality of memory cells disposed on a first and second level;

the memory cells on the first level being coupled to first lines and common lines; and

the memory cells on the second level being coupled to second lines and the common lines.

9. The array defined by claim 8, wherein each memory cell comprises a diode and a breached antifuse layer when programmed.

10. The array defined by claim 9, wherein the first lines are disposed above the common lines and the second lines are disposed below the common lines.

11. A memory disposed above a substrate comprising:

a plurality of memory levels organized as first alternate levels disposed between second alternate levels;

a plurality of two terminal memory cells incorporated into each of the levels;

one terminal of the cells in each of the first alternate levels and each of the second alternate levels being coupled to first lines shared by the cells in each pair of first and second alternate levels;

the other terminal of the cells in each of the first alternate levels being coupled to second lines; and

the other terminal of the cells in each of the second alternate levels being coupled to third lines.

12. The memory defined by claim 11, wherein each cell comprises, when programmed, a diode and an antifuse layer.

13. The memory defined by claim 12, wherein the diodes comprise an N- region and a P+ region.

14. The memory defined by claim 13, wherein the N- regions in the diodes in at least one of the first and second alternate levels has a smaller cross-section than the P+ region.

15. The memory defined by claim 12, wherein the antifuse layer comprises silicon dioxide.

16. The memory defined by claim 14, wherein the antifuse layer comprises silicon dioxide.

17. The memory defined by claim 13, wherein the diodes include polysilicon layers.

18. The memory defined by claim 17, wherein the polysilicon layers include an N- layer and a P+ layer.

19. The memory defined by claim 18, wherein the first, second, and third lines comprise a silicide.

20. The memory defined by claim 19, wherein the silicide comprises titanium silicide.

21. The memory defined by claim 20, wherein the shared first lines contact the P+ layers.

22. A memory disposed above a substrate comprising:

a plurality of memory levels organized as first alternate levels disposed between second alternate levels;

a plurality of two terminal memory cells incorporated into each of the levels;

one terminal of the cells in each of the first alternate levels and each of the second alternate levels being coupled to first lines shared by the cells in each pair of first and second alternate levels;

the other terminal of the cells in each of the first alternate levels being coupled to second lines;

the other terminal of the cells in each of the second alternate levels being coupled to third lines; and

an oxide layer disposed between each of the pair of first and second alternate levels.

23. The memory defined by claim 21, wherein each cell comprises, when programmed, a diode and a breached antifuse layer.

24. The memory defined by claim 23, wherein at least some of the diodes comprise two regions, one having a smaller cross-section than the other.

25. A memory disposed above a substrate comprising:

a plurality of memory levels, each level having a plurality of two terminal memory cells;

each of the memory cells comprising a diode and a breached antifuse layer, when programmed;

one terminal of the cells in first alternate levels and second alternate levels of the memory levels being coupled to first lines, shared by the cells;

the other terminal of the cells in the first alternate levels being coupled to second lines in each of the first alternate levels; and

the other terminal of the cells in the second alternate levels being coupled to third lines in each of the second levels,

such that cells in paired first and second alternate levels are coupled to shared first line and one of the second and third lines.

26. The memory defined by claim 25, wherein at least some of the diodes have two regions one of which has a smaller cross-section than the other.

27. In a three-dimensional memory array, two adjacent memory levels comprising:

a first plurality of parallel, spaced-apart rail-stacks;

a second plurality of parallel, spaced-apart rail-stacks perpendicular to the first rail stacks disposed above the first rail-stacks;

a third plurality of parallel, spaced-apart rail-stacks perpendicular to the second rail-stacks disposed above the second rail-stacks, the first, second, and third rail-stacks being of approximately the same height;

the first rail-stacks and a first portion of a second rail-stacks defining first cells in one of the two levels and the third rail-stacks and a second portion of the second rail-stacks defining second cells in the other level of the memory, and

the third rail-stacks including conductors shared by the first and second cells.

28. The array of claim 27, wherein each cell comprises a diode and a breached antifuse layer, when programmed.

29. The array of claim 28, wherein each diode includes a P+N- junction.

30. The array of claim 29, wherein the antifuse layer of the cells comprises silicon dioxide.

31. A process for fabricating two memory levels in a memory array comprising:

forming a first conductive layer;

depositing a first semiconductor layer over the first conductive layer, the first semiconductive layer being doped with a first conductivity type dopant;

etching the first conductive layer and the first semiconductor layer into a plurality of first parallel, spaced-apart rail-stacks;

filling the space between the first rail-stacks with a first insulator;

planarizing the first upper surface of the first rail-stacks and the first insulator;

forming a first antifuse layer over the planarized first upper surface;

depositing a second semiconductor layer doped with a second conductivity type dopant over the first antifuse layer;

forming a second conductive layer over the second semiconductor layer;

depositing a third semiconductor layer doped with a second conductivity type dopant over the second conductive layer;

etching the second semiconductor layer, second conductive layer, and third semiconductor layer into a plurality of second parallel, spaced-apart rail-stacks;

filling the space between the second rail-stacks with a second insulator;

planarizing the second upper surface of the second insulator and the second rail-stacks;

forming a second antifuse layer on the planarized second upper surface;

depositing a fourth semiconductor layer doped with a first conductivity type dopant over the second antifuse layer;

forming a third conductive layer;

etching the third semiconductor layer and third conductive layer to form third parallel, spaced-apart rail-stacks;

filling the space between the third rail-stacks with a third insulator.

32. The process defined by claim 31, wherein the first, second, third, and fourth semiconductor layers comprise polysilicon layers.

33. The process defined by claim 31, wherein the first conductivity type is N type, and the second conductivity type is P type.

34. The process defined by claim 33, wherein the N type polysilicon layers are doped to a concentration level of N-, and the P type polysilicon layers are doped to a concentration level of P+.

35. The process defined by claim 31, wherein the first and second antifuse layers comprise silicon dioxide.

36. The process defined by claim 31, wherein the first, second, and third rail-stacks have approximately the same height.

37. The process defined by claim 31, wherein the first, second, and third conductive layers comprise a silicide.

38. The process defined by claim 37, wherein silicon is deposited on a metal layer to form the silicide.

39. A process for fabricating two memory levels in a memory array comprising:

forming a first conductive layer;

depositing a first semiconductor layer over the first conductive layer, the first semiconductive layer being doped with a first conductivity type dopant;

etching the first conductive layer and the first semiconductor layer into a plurality of first parallel, spaced-apart rail-stacks;

filling the space between the first rail-stacks with a first insulator;

planerizing the first upper surface of the first rail-stacks and the first insulator;

forming a first antifuse layer over the planarized first upper surface;

depositing a second semiconductor layer doped with a second conductivity type dopant over the first antifuse layer;

forming a second conductive layer over the second semiconductor layer;

depositing a third semiconductor layer doped with a second conductivity type dopant over the second conductive layer;

depositing a fourth semiconductor layer doped with a first conductivity type dopant over the third semiconductor layer;

etching the second semiconductor layer, second conductive layer, third semiconductor layer and fourth semiconductor layer into a plurality of second parallel, spaced-apart rail-stacks and an etched fourth semiconductor layer;

filling the space between the second rail-stacks and the etched fourth semiconductor layer with a second insulator;

planerizing the second upper surface of the second insulator and the etched fourth semiconductor layer;

forming a second antifuse layer on the planarized second upper surface;

forming a third conductive layer;

etching the third conductive layer and etched fourth semiconductor layer to form third parallel, spaced-apart rail-stacks;

filling the space between the third rail-stacks with a third insulator.

40. The process defined by claim 39, wherein the first, second, third, and fourth semiconductor layers comprise polysilicon layers.